| **Work package number** | WP26 | **Start date** | 01/01/2012 |
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| **Activity Type** | RTD | | |
| **Work package acronym** | ULISINT | | |
| **Work package title** | Integration of ultra-light silicon tracking and vertex detection systems for frontier precision experiments | | |

| **Beneficiary number** | **Organization legal name** *(in italics the Research Units)* | **Short name** | **Activity leaders** *(in **bold** the spokesperson)* | **Human effort**[1] (see note below) *(person-months)* |
|---|---|---|---|---|
| 12 | GSI Helmholtzzentrum fuer Schwerionenforschung GmbH | GSI | **J. Heuser** | 6 (36) |
| 1 | Istituto Nazionale di Fisica Nucleare<br>*INFN Sezione di Torino* | INFN<br>*INFN-TO* | <br>*A. Rivetti* | 18 (36)<br>*18 (36)* |
| 13 | Johann Wolfgang Goethe Universitaet Frankfurt am Main | GUF | J. Stroth | 4 (36) |
| **Other involved institutions not receiving EC funds** | | | **Activity leaders** | **Estimated human effort involved in the WP** |
| Kiev Institute for Nuclear Research (KINR), National Academy of Science of Ukraine (NASU) (Ukraine) | | | V. Pugatch | (6) |
| State Enterprise Scientific Research Technological Institute of Instrument Engineering (SE SRTIIE) (Ukraine) | | | V. Borshchov | (6) |
| Interuniversity Microelectronic Centre (IMEC) (Belgium) | | | P. De Moor | (6) |

## *1. OBJECTIVES*

Frontier precision hadron physics experiments are being prepared at the international research facility FAIR (CBM and PANDA detectors), at BNL (upgrades of the PHENIX and STAR detectors), at the LHC (upgrades to the ALICE detector) and at the CERN SPS (new fixed-target experiments either already under development or under study). Their physics programmes address detailed investigations of the properties of hadrons in a nuclear medium as well as the microscopic properties of matter under extreme conditions of temperature and density. Special emphasis of the next generation experiments is to highest sensitivity in the reconstruction of rare probes. The physics leads to the experimental task of reconstructing nuclear interactions at unprecedentedly high rates, each generating high particle multiplicities in which rare probes or their decay particles are occasionally embedded. The reconstruction of the events requires large-area thin silicon detectors for high-resolution momentum determination (of the order of 1%) in a tracking system, and high-precision decay vertex identification of rare short-lived decays (e.g. of D mesons or of the $\Lambda_c$ baryon) in a micro-vertex detector, operating efficiently at interaction rates up to 20 MHz.

Current state-of-the-art large-area silicon detector systems like those that are now operational in high-energy physics and heavy-ion physics experiments at the LHC are based on developments at the industrial technical limit dating back up to 10 years. Despite of their sophistication, they are largely insufficient for

[1] *The numbers provided indicate the human effort in person-months to be justified to the EC as costs of the project: EC funds + home contribution.*
*The numbers in brackets indicate the total estimated human effort engaged in the WP (project + extra home contribution).*
*No number given outside the brackets means that the beneficiary does not receive EC funds in that WP.*
*0 (zero) outside the brackets means that the beneficiary does not receive EC funds for personnel in that WP.*

the new research programmes in hadron physics in particular what concerns the material budget of the full detector system, comprising much more material than the (usually reasonably thin) sensing part alone, namely the mechanical support and the front-end electronics section with its unavoidable cooling infrastructure.

In the preceding research activity ULISI of HadronPhysics2, we have been exploring new concepts and technologies fulfilling the requirements of the next-generation hadron physics experiments. We covered three fields of large-area tracking and vertex detectors, each of them backbones of the upcoming CBM and PANDA detectors at FAIR: (a) a thin fast micro-strip tracking detector system for large area coverage, (b) a thin fast pixel hybrid detector system for tracking in very high particle densities, and (c) an ultra-thin monolithic pixel detector system with very high spatial resolution for decay vertex identification. For all three applications, the research effort has been focused on the sensing part of the system, in particular its mass-minimization, and a low-mass bridge towards the readout electronics and services end. The solution for the micro-strip based tracking system is to mount double-sided sensors onto a high-performance carbon fiber support and to rout the sensor signals through ultra-low mass micro-line cables to front-end electronics to be placed at the periphery of a modular ladder structure. For the hybrid pixel detector, a mass-optimized hybrid assembly of a low-power readout chip and a thin epitaxial pixilated sensor has been produced. The demonstrator for the micro-vertex detector pioneers a novel ultra-thin array of thinned monolithic pixel detectors, wrapped into a foil-like bus layer or mounted on a thin bus substrate.

The research activity ULISINT proposed here for HadronPhysics3 builds on these developments and shall complete the exploration of technologies and procedures towards the integration of the three types of detectors into full systems. Several key issues to be solved are common to all of them and include:

- Realization of high-density readout sections with compact arrangement of front-end chips and services like power supplies and data links.
- Implementation of power management and data transmission schemes that minimize the need of off-chip components (filtering capacitors and interconnects).
- Heat evacuation from the thin detector system or its readout section.
- Mixed-atmosphere interface (sensing part in thermal enclosure or vacuum, readout section outside of the thermal barrier, insulation and feed-through of services).
- Layouts and materials compatible with mass production (industrialization) of components.
- Related assembly and handling procedures of thin double-sided segmented objects.
  They are addressed in three tasks, one for each type of detector system, which are described in the next chapter.

## *2. DESCRIPTION OF WORK AND ROLE OF PARTICIPANTS*

| **Task** | **Title** | **Participants** |
|---|---|---|
| 1 | Integration of a low-mass large-area silicon micro-strip detector system for particle tracking. | GSI |
| 2 | Integration of a low-mass silicon pixel detector system for particle tracking. | INFN-TO |
| 3 | Integration of a flexible, silicon embedded sensor assembly into a prototype pixel ladder for micro-vertex detection. | GUF |
| Task 1<br>***Integration of a low-mass large-area silicon micro-strip detector system for particle tracking****: development of a high-density front-end electronics board for the readout of an ultra-light large-area silicon micro-strip tracking system; exploration of technologies for their mass-production; definition of procedures and tools for their assembly into tracking detector modules; definition of procedures for the module integration into the mainframe/thermal enclosure of the CBM micro-strip tracking system.* | | |

| Sub-task | Title | Participant |
|---|---|---|
| 1.1 | Provision of ultra-light Aluminum-Kapton micro-strip readout cables for bonding tests on various FEB substrates. | GSI, SE SRTIIE |
| 1.2 | Design and production of high-density input patterns on various FEB substrates. | GSI |
| 1.3 | Investigation of thermal, mechanical and electrical quality of the substrates, metal structuring quality, and TAB-bonding of cables to the substrates. Definition of the FEB basis material. | GSI, SE SRTIIE |
| 1.4 | Development and production of a demonstrator FEB with several CBM-specific prototype readout chips. | GSI |
| 1.5 | Development and production of a demonstrator FEB with full integration of readout chips and services for power supply, data links and controls. | GSI |
| 1.6 | Development and production of the demonstrator of a fully integrated FEB, including high-density input stage. | GSI |
| 1.7 | Evaluation of the FEBs on test stands; TAB-bonding of sensor-cable assemblies to FEB demonstrators. | GSI, SE SRTIIE, KINR |
| 1.8 | Definition of procedures for the mass-production of FEBs; definition of procedures and tools for the assembly of multi-sector micro-strip detector modules; solutions, procedures and tools for their integration into the mainframe of the CBM micro-strip tracking detector system, with focus on efficient cooling of the readout section, thermal insulation of readout and sensing sections while enabling feed-throughs of signal cables and reworkability. | GSI, SE SRTIIE, KINR |

Task 2

***Integration of a low-mass silicon pixel detector system for particle tracking****: a key towards the minimization of material budget in hybrid pixel systems is the reduction of external components and service chips that present-day front end for pixel detectors need for a correct operation. On chip cap-less regulators that avoid external filtering capacitors are employed in chips for mobile phones and other commercial System on Chips, but their use in particle detectors front-end, where the specifications on noise and radiation hardness are particularly demanding, remain to be assessed. Low-power transmitter coupled to ultra-light aluminum based cables allowing high speed electrical transmission over moderate distances (a few meters) would also be useful to avoid extra electro-optical components in zones where the material budget must be minimized. The design of such components and their integration on a realistic front-end demonstrator is therefore the natural complement to the low-power front-end cells with increased functionality developed in the ULISI project. Based on this chip, a full low-mass module prototype will be developed in ULISINT proposal.*

| Sub-task | Title | Participant |
|---|---|---|
| 2.1 | Development of low-power radiation-tolerant power regulators and data transmitters to be embedded on pixel front-end ASIC. | INFN-TO |
| 2.2 | Development of low-mass, fine pitch Al cables for off-chip electrical transmission. | INFN-TO |
| 2.3 | Design and test of a full front-end ASIC incorporating the circuits developed in 2.1. | INFN-TO |
| 2.4 | Design of a low-mass front-end module based on the ASIC and cables developed in 2.2, 2.3. | INFN-TO |

Task 3

***Integration of a flexible, silicon embedded sensor assembly into a prototype pixel ladder for micro-vertex detection****: placement of the active part of the detector onto a support structure with high precision, achieving excellent heat evacuation and sufficient rigidity; exploration of alternative approach as fall*

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|---|---|---|
| *back solution if the new technology will not be available in time. Evaluation of technologies allowing reducing the inactive area between individual sensor chips.* | | |
| Sub-task | Title | Participant |
| 3.1 | Evaluation of the mechanical and electrical properties of a prototype silicon embedded chip assembly. | GUF, IMEC |
| 3.2 | Test series to study the suitability for operation in vacuum and under cryogenic operation. | GUF |
| 3.3 | Preparation of CVD diamond or TPC/RVC compound support structures. | GUF |
| 3.4 | Design of the prototype chip assembly. Placement of the sensor chip and design of the electrical interconnection lines. | GUF, IMEC |
| 3.5 | Integration of the prototype assembly into the detector ladder. | GUF, IMEC |

## *3. DELIVERABLES BRIEF DESCRIPTION*

1. Report on full-size high-density front-end board compatible with the integration requirements into the CBM silicon micro-strip tracking system, in a technology available for mass-production.

2. Report on the feasibility of cap-less front-end ASIC, the performance of a low-power, low-mass high speed transmission system based on Al cable, and the design of a final full-size front-end module.

3. Report on the performance of the prototype ladder under test beam. Summary of design specifications and guidelines for the design of the final micro vertex detector.

## *4. EXPECTED IMPACT*

All three silicon detector technologies are backbones for the experiments at FAIR.

The development of their components and integration compatibility into large-scale systems has therefore high impact on the physics programmes at FAIR, but also at programmes underway or planned at other hadron colliders at CERN. Examples are the planned upgrades of the ALICE inner tracking system with additional silicon pixel detector layers, or the outfitting of fixed-target experiments with new tracking devices.

The development of components at the limit of commercial availability, e.g. printed circuit boards with fine-structuring of the metallization layers near 50 μm, requires close cooperation with industry to achieve readiness for mass production. Our application represents a technological push for high-technology enterprises in Europe.

With decreasing feature size of CMOS processes sensor/readout chip assemblies with even improved single point position resolution have become available. This progress asks for new integration techniques to match the material budget with the improved sensor performance. At the same time the power density is rising due to the higher integration density of the electronics and low-mass heat evacuation concepts are more and more crucial for the design. Successful integration concepts will find their application in other experiments where high-precision vertexing is required.